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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,193	12/01/2003	Stephen K. Sunter	LVPAT064US	1340

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,193	SUNTER, STEPHEN K.	
	Examiner	Art Unit	
	Toan M. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,9 and 10* is/are rejected.

7)☒ Claim(s) *2-8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sunter et al. (U.S. Patent No. 5,659,312).

Referring to claim 1, Sunter et al. disclose a method for deducing parameters of data signals, comprising:

generating data signals using predetermined data sequences (col. 8, lines 24-26; col. 9, lines 37-38);

measuring average voltage of each said data signals (col. 8, lines 30-42; col. 10, lines 12-13); and

deducing said parameters from said average voltages (col. 8, lines 59-65; col. 10, lines 14-16).

As to claim 9, Sunter et al. disclose a method for of testing a digital circuit, comprising deducing parameters as defined in claim 1 and comparing deduced parameter values against expected parameter values to determine whether said digital circuit passes or fails (col. 6, lines 39-47).

Referring to claim 10, Sunter et al. disclose a method of testing an analog circuit, comprising deducing parameters as defined in claim 1 and comparing deduced parameter values

against expected parameter values to determine whether said analog circuit passes or fails (col. 6, lines 39-47).

Claims 2-8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claims 2 and 11 is the inclusion of deducing the parameters being logic voltages and rise and fall times and comparing the deduced logic voltages and rise and fall times of the circuit output signal to that of the circuit input signal to determine circuit gain and frequency response.

The reason for allowance of the claims 3-4 is the inclusion of the steps of measuring average voltage for a periodic pattern containing a number of consecutive same-value logic values and a pattern containing a different number of consecutive same-value logic values for deducing the difference between two logic levels and comparing the measured average voltage to an expected average voltage to produce an acceptable difference between the two logic levels.

The reason for allowance of the claims 5-6 is the inclusion of the steps of measuring average voltage for a periodic pattern containing a number of consecutive same-value logic values and a pattern in which the number of consecutive same-value logic values are split in two or more groups of same-value logic values for deducing the difference between effective rise and fall transition times and comparing the measured average voltage to an expected average voltage to produce an acceptable difference between effective rise and fall transition times.

The reason for allowance of the claims 7-8 is the inclusion of the steps of measuring average voltage for a periodic pattern containing a number of consecutive same-value logic

values and a pattern containing a different number of consecutive same-value logic values, in which the number of consecutive same-value logic values is split into two or more groups of same-value logic values, and a pattern containing one or more isolated logic values surrounded by the opposite logic value for obtaining rise and fall transition times and comparing the measured average voltage to an expected average voltage to produce an acceptable rise and fall transition times.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"A 4-GHz Effective Sample Rate Integrated Test Core for Analog and Mixed-Signal Circuits", Hafed et al., IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, April 2002, Pages 499-514

"A Digital Partial Built-In Self-Test Structure for a High Performance Automatic Gain Control Circuit", Lechner et al., Design Automation and Test Europe Conference, 9-12 March 1999, Pages 232-238

"Investigations of Mixed-Signal Circuits Equipped with Innovative Test Bus", Borkowska et al., 1999 IEEE, Pages 1553-1557

"Differential-Line-Scheme of Clock and Signal Bus of High-Speed Digital Circuits and Systems for Minimizing Electromagnetic Radiated Emission", Kim et al., 1998 IEEE, Pages 860-865

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

May 9, 2005

John Barlow
Supervisory Patent Examiner
Technology Center 2800